UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,073	01/23/2001	William Frederick Sauber	16356.573 (DC-02636)	2498

27683 7590 03/11/2003

HAYNES AND BOONE, LLP
901 MAIN STREET, SUITE 3100
DALLAS, TX 75202

EXAMINER	
NGUYEN, HAU H	
ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 03/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/768,073	SAUBER, WILLIAM FREDERICK	
	Examiner	Art Unit	
	Hau H Nguyen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-3, 5, 7-12, 14, 16-19, 21 are rejected under 35 U.S.C. 102(a) as being anticipated by Yamaki (U.S. Patent No. 5,072,411).

Referring to claim 1, Yamaki teaches a computer system to which display controllers of a plurality of types, such as those which may use a CGA (color graphics adapter) mode, an EGA (enhanced graphics adapter) mode, and a VGA (video graphics array) mode, are connectable (col. 1, lines 7-11). As shown in FIG. 1, Yamaki teaches a central processing unit (CPU) 1, read only memory (ROM) 2, manual switch 4, random access memory (RAM) 6, and optional display controller 5 (second video controller) are connected to system bus 11. Built-in display controller 3 (first video controller), having a conventional, well-known, structure is connected to system bus 11 through manual switch 4 (a switching device). The above-mentioned components can be centrally arranged within a main body. Plasma display 9, which is provided within the main body of the computer system, is connected to built-in display controller 3. Cathode ray tube (CRT) 10 (display device), which may be used as an external display remote from the main body, is connectable to optional display controller 5 (col. 2, lines 35-47). Yamaki further teaches either built-in display controller 3 (hereafter "DC 3") or optional display

controller 5 (hereafter "DC 5") is selected beforehand by the user by means of switch 4 (col. 3, lines 31-33).

In regard to claim 2, as cited above, Yamaki teaches the display controller 3 (first video controller) is a built-in display controller, and the built-in display controller 3 is centrally arranged within a main body, which implies a chipset.

Referring to claim 3, Yamaki further teaches the optional display controller 5 may be located either inside or outside of the main body of the system (col. 3, lines 19-20). With reference to Fig. 1, the optional display controller 5 is coupled to the chipset.

As for claim 5, as cited above, Yamaki teaches the components (including the built-in display controller 3 and the switch 4 can be centrally arranged within a main body (col. 2, lines 41-42).

In regard to claims 7-9, with reference again to Fig. 1, Yamaki teaches plasma display 9 (first display device), which is provided within the main body of the computer system, is connected to built-in display controller 3. Cathode ray tube (CRT) 10 (second display device), which may be used as an external display remote from the main body, is connectable to optional display controller 5 (col. 2, lines 35-47). Yamaki further teaches that either built-in display controller 3 (hereafter "DC 3") or optional display controller 5 (hereafter "DC 5") is selected beforehand by the user by means of switch 4 (col. 3, lines 31-33). Thus, it is inherent that the switch should be coupled with a first and second connector to receive a first and second display.

Referring to claims 10, 19, and 21, as cited above, Yamaki teaches a computer system having a first video controller 3, a second video controller 5, and a switching device 4. Yamaki further teaches when this switch 4 is on, identifier information in the

EGA BIOS stored in ROM 31 of built-in display adapter 3 can be read. When the switch is off, the identifier information cannot be read (col. 2, lines 61-64). The operation of the system is described with reference to Fig. 4. First, at step 402 of the CPU 1 attempts to read the identifier information written in the BIOS of built-in DC 3, so as to determine whether, built-in DC 3 or optional DC 5, has been selected by the user. If the identifier information can be read (second video controller is not coupled to the interface), built-in DC 3 (first video controller) is regarded as having been selected. Accordingly, the system is actuated with built-in DC 3 at step 404. If the identifier information cannot be read (second video controller is coupled to the interface), optional DC 5 (second video controller) is regarded as having been selected (col. 3, lines 40-49).

In regard to claim 11, as cited above, Yamaki teaches the display controller 3 (first video controller) is a built-in display controller, and the built-in display controller 3 is centrally arranged within a main body, which implies a chipset.

Referring to claim 12, Yamaki further teaches the optional display controller 5 may be located either inside or outside of the main body of the system (col. 3, lines 19-20). With reference to Fig. 1, the optional display controller 5 is coupled to the chipset.

As for claim 14, as cited above, Yamaki teaches the components (including the built-in display controller 3 and the switch 4 can be centrally arranged within a main body (col. 2, lines 41-42).

In regard to claims 16-18, with reference again to Fig. 1, Yamaki teaches plasma display 9 (first display device), which is provided within the main body of the computer system, is connected to built-in display controller 3. Cathode ray tube (CRT) 10 (second display device), which may be used as an external display remote from the main body, is

connectable to optional display controller 5 (col. 2, lines 35-47). Yamaki further teaches that either built-in display controller 3 (hereafter "DC 3") or optional display controller 5 (hereafter "DC 5") is selected beforehand by the user by means of switch 4 (col. 3, lines 31-33). Thus, it is inherent that the switch should be coupled with a first and second connector to receive a first and second display.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6, 15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaki (U.S. Patent No. 5,072,411) in view of Westberg et al. (U.S. Patent No. 4,862,156).

Referring to claims 6, 15 and 20, as shown in Fig. 1, Yamaki teaches CPU 1 (a processor) controls the operation of the computer system. ROM 2 (system memory) stores a Basic Input Output System (system BIOS) which is a program to control the inputs and outputs of the computer system. The system BIOS input/output controls the execution of programs which enable operation at input and output devices connected to a system (col. 2, lines 48-54). Thus, Yamaki teaches all the limitations of claims 6, 15 and 20, except for the program includes instructions for causing the switching device to provide the first signal or the second signal to the first display device.

However, Westberg et al. teach a dual-mode video computer system which is capable of executing at least two different types of graphics programs designed for at least two different graphics controllers (col. 2, lines 41-45). As show in Fig. 2, Westberg et al. teach a video computer system (VCS) comprising a first video graphics controller 18, a second video graphics controller 19. The microprocessor 10 generates a signal 30 which selects the appropriate graphics controller 18, 19 to compatibly execute the particular type of graphics program presented to the VCS. The signal 30 also instructs select means 26 (switching device) in order to select the appropriate output from either the first video graphics controller 18 or the second video graphics controller 19 to be input to the RF modulator 22 (col. 4, lines 13-29).

Therefore, it would have been obvious to one skilled in the art to utilize the method of programming the selector as taught by Westberg et al. in combination with the computer system as taught by Yamaki in order to automatically identify the type of graphics program presented to the system and which correspondingly selects the compatible graphics controller to execute the program (col. 2, lines 47-51).

5. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaki (U.S. Patent No. 5,072,411) in view of Behrbaum et al. (U.S. Patent No. 6,326,973).

Referring to claims 4 and 13, as cited above, Yamaki teaches all the limitations of claims 4 and 13, except for the chip set includes an AGP port.

However, Behrbaum et al. teach a computer system using at least one accelerated graphics port (AGP) with at least two core logic chip sets, and more particularly, in allocating AGP/GART memory from the system memory local to the AGP device (col. 1,

lines 26-30). As shown in FIG. 4, the computer system 400 has two core logic units 404a and 404b (chip sets). A graphics controller 410 is connected to the AGP bus 413, which, in turn, is connected to the AGP request and reply queues 411 that link the AGP bus 413 to the host bus 403 and the first memory controller 464a (col. 10, lines 7-10, and 14-18).

Therefore, it would have been obvious to one skilled in the art to utilize the method of incorporating an accelerated graphics port to the chip sets as taught by Behrbaum et al. in combination with the computer system as taught by Yamaki in order to obtain a low-cost and high speed access to graphics data stored in memory (col. 2, lines 54-61).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892 form.

Hawkins et al. (U.S. Patent No. 6,304,244) disclose a method and system for dynamically selecting video controllers present within a computer system.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

0 0 0 0 0
0 0 0 0 0
0 0 0 0 0

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600